

REMARKS

This Amendment is a full and timely response to the Office Action dated April 26, 2004. Reexamination and reconsideration are respectfully requested.

Claim for Priority

It is noted with appreciation that the Action acknowledges receipt of the priority document in support of the claim for foreign priority.

Drawings

It is noted with appreciation that the drawings are accepted by the Examiner. However, errors were noted in Fig. 3 and have been corrected herewith.

Specification

The specification has been reviewed and amendments have been made to the specification view of the indication of allowable subject matter to prepare this application for final printing. However, in reviewing the specification and drawings for final printing in that allowable subject matter is indicated, minor errors in the sheet containing Figs. 3A to 3J were noted, and a request for submission of corrected drawings provided.

Abstract of the Disclosure

The Abstract of the Disclosure has been amended to include, among other things, text addressing the criticism made by the examiner for use of the word "comprising". The Abstract is submitted as a separate page, according to the preferred practice for these changes.

Title of the Invention

The title of the invention was not apt. The new title proposed is: --CLOCKING SWITCHING CIRCUIT FOR SWITCHING FROM ONE TO ANOTHER DIFFERENT CLOCK SIGNAL WITHOUT HAZARD--. If the examiner persists in his critique of this title, he is invited to propose another to his liking.

Objections to claims

Claims 1, 2 and 5 were objected to for what seem primarily to be inconsistencies in the use of certain terms. Claim 1 has been revised in a way that permits incorporation of the examiner's suggestions, or an alternative that is consistent. Accordingly, it is submitted that this objection may be withdrawn

Claims 1 to 6 as Indefinite

Claims 1 to 5 were initially rejected as allegedly being indefinite. Claim 1 has been amended to overcome this formal rejection by clarifying that the clock switching circuit that is the subject of this invention receives as an input a plurality of clock signals including a first clock signal and a second clock signal. The subject circuit switches one clock signal to be output from the first clock signal to the second clock signal. The circuit includes a plurality of switching circuit respectively receiving said clock signals, associated selection signals of the clock signals, and an enabling signal, so that the unit circuit controls and stops the clock signals in accordance with the selection signals and the enabling signal. See Fig. 1, and especially Fig. 3 where Figs. 3A and 3B show the first and second clock signal, Figs. 3C and 3D show the associated selection signal, Figs. 3E and 3F show the output condition monitor signals, Fig. 3G shows the enabling signal, and Figs. 3H and 3I show during the period T3 to T5 that both clock output signals are off. The composite output signal is shown in Fig. 3J. It is submitted that the revised claim 1 reads on this operation, as described in the specification at pages 13, line 3 to page 19, line 23.

The helpful suggestions and observations by the examiner are acknowledged with appreciation. In particular, the suggestions as to claims 3 and 5 are adopted.

Claims 1 to 5 as Allegedly Anticipated by Pasqualini; Claim 6 allowable

Upon revision of claims 1 to 5 to overcome the alleged indefiniteness noted by the examiner, claim 1 is amended to include the subject matter of allowable claim 6. Thus the rejection of claims 1 to 5 is mooted. Newly-added claims 6 to 10 are thus also allowable as

dependent on allowable amended claim 1.

To the extent that the allowed claims 1 to 5 and 7 to 10 may arguably read on Fig. 7, new claims 11 to 20 are added in a means plus function format to provide coverage of the the embodiments of Figs. 1 to 6 as well. Specifically, Pasqualini uses a logic circuit 611, as selected by the examiner, for sampling a high to low transission of CLKOUT, whereas for a two signal transition shown in the Applicant's Figs. 3H and 3I, both CLKOUT signals are low during a period of transition after enablement (Fig. 3G) between T3 to T5 due to the delay affect of the delay unit. Thus the Applicant's circuit functions differently from Pasquallini. The examiner's explicit citation in these respects is appreciated, and may be the result of a question of the operation of the last five lines of original claim 1. With the explanation above for the Applicant's Figs. 1 and 3, in contrast to col. 7, lines 13 to 32 of Pasqualini and Fig. 7 thereof, claim 11 is believed to be allowable over Pasqualini.

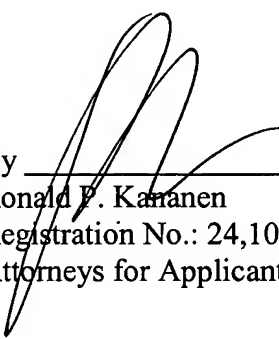
It should be noted that Pasqualini requires that the SELECT signals be synchronized and change value on the rising edge of CLKOUT. With the use of the Applicant's delay unit, as shown in Fig. 2, the Applicant's circuit is not so limited. In short, therefore, Pasqualini builds in a delay by logic by holding CLKOUT low, whereas the Applicant's circuit uses the delay unit not shown or described as a unit in Pasqualini.

Finally, it is observed that the examiner does not contend that the unit circuit alleged equivalent in circuits 601, 602, and 603 include delay circuits as now recited in newly-added claim 11. Thus, Pasqualini is deficient in meeting the terms of this claim.

In the event that the Examiner has any comments or suggestions which could place this application in even better form, the Examiner is invited to telephone the undersigned attorney at the below-listed number.

Respectfully submitted,

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By 
Ronald F. Karanen
Registration No.: 24,104
Attorneys for Applicant

RADER, FISHMAN & GRAUER, PLLC

Lion Building
1233 20th Street, N.W., Suite 501
Washington, D.C. 20036
Tel: (202) 955-3750
Fax: (202) 955-3751

Customer No. 23353

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